REMARKS

Claims 1-9, 12, 14-15 and 20-22 were pending in the application. Claims 20-22 have been cancelled. Accordingly, claims 1-9, 12, and 14-15 remain pending in the application. Reconsideration is respectfully requested in view of the amendments to the claims and the following remarks. Reconsideration is respectfully requested in view of the amendments to the claims and the following remarks.

I. The § 112 Rejections

Claims 20-22 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. In particular, the Examiner asserts that even though the concept of altering the debug client function to debug software is disclosed in the specification on page 7, line 20 to page 8, line 5, there is not sufficient detail to enable one of skill in the art to make or use the invention. Applicant has cancelled claims 20-22 rendering this rejection moot. Nevertheless, Applicant respectfully disagrees with the Examiner's assertion that only the concept of altering the debug client function to debug software is disclosed. The specification discloses two specific techniques for altering the debug client function to debug software – 1) using the debug client function to manage instruction pointer logic within an ASIC, and 2) using the debug client function to manipulate registers and memory. Applicant respectfully submits that such a disclosure provides sufficient detail for one of skill in the art to make (or use) the invention.

II. The § 103 Rejections

Claims 1-9 and 12-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent. 6,829,751 ("Shen").

Applicant respectfully traverses the rejections.

Claim 1 recites an application specific integrated circuit (ASIC) including a field programmable gate array (FPGA) coupled to a plurality of internal signals (including at least one bus) within the ASIC. The FPGA includes a debug client function that is in communication with a server and includes comparator logic operable to compare selected ones of the plurality of internal signals coupled to the FPGA with a trigger pattern downloaded from the server, and includes storage logic operable to store a state of the selected ones of the plurality of internal signals that match the trigger pattern for later retrieval by the server.

A. Shen Fails To Disclose an FPGA having a Debug Client Function That Includes Comparator Logic Operable To Compare Selected Ones of a Plurality of Internal Signals Coupled to the FPGA with a Trigger Pattern Downloaded from a Server

Shen discloses a system for designing an integrated circuit (IC) (see Abstract). More specifically, Shen discloses implementing an FPGA core that may be used to perform on-chip diagnostics that enable debugging functions, such as bus monitoring, probing, single step running, triggering, and capturing (col. 2, ll. 39-45).

The Examiner acknowledges that Shen fails to explicitly disclose an FPGA containing a debug client function including comparator logic operable to compare selected ones of a plurality of internal signals coupled to the FPGA core with a trigger pattern downloaded from a server. However, the Examiner asserts that because Shen teaches monitoring the correctness of a bus protocol, detecting errors, and verifying bug fixes, then it would have been obvious to one of skill in the art that Shen possesses the claimed comparator logic. Further, the Examiner asserts that the functions of monitoring, verifying bug fixes, and detecting errors cannot be accomplished without "comparator logic operable to compare selected ones of a plurality of internal signals coupled to the FPGA core with a trigger pattern downloaded from a server". Applicant respectfully disagrees.

While Shen discloses performing the functions of monitoring, verifying bug fixes, and detecting errors, Applicant submits that these functions are performed by the debugging workstation (or circuit) 104 (working with the FPGA core 106), which debugging workstation 104 is not contained within the FPGA core 102 (see col. 2, ll. 63-65; FIG. 1). That is, Shen discloses that data is collected from the FPGA core and sent to the debugging workstation where the internal signals are analyzed (col. 3, ll. 52-57; col. 4, ll. 55-58). Accordingly, because Shen discloses performing error detection using the debugging workstation 104, Shen, therefore, teaches away from including comparator logic (as recited in claim 1) within an FPGA. Prior art references must be considered in their entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983).

B. Shen Fails To Disclose an FPGA Having Storage Logic Operable To Store a State of Selected Ones of a Plurality of Internal Signals That Match The Trigger Pattern For Later Retrieval By a Server

In operation, Shen's FPGA core 116 (FIG. 3) is used to collect data from registers using a scan chain (col. 3, ll. 36-41). In particular, a user decides which signals need to be observed during a debugging period and, accordingly, the FPGA generates select signals (e.g., DIAG_SEL10 and DIAG_SEL11) that control which scan segments (of the scan chain) need to be accessed (col. 5, ll. 30-33; col. 4, ll. 35-58). After data is collected from the scan chains, the data is compressed and sent to a debugging workstation (col. 3, ll. 52-54). Thus, Shen discloses storing only signals within the FPGA core 116 that are pre-selected by a user, and not signals that match a trigger pattern.

In addition, while Shen discloses that the system 100 is operable to search for a specific signal pattern (see col. 6, l. 11), Shen is silent as to specifically *how* the signal pattern is

searched. Based on the above, Applicant respectfully submits that Shen's debugging workstation 104 performs the function of searching for a specific signal pattern based on data collected from the FPGA core 116. Thus, Shen fails to disclose storage logic operable to store a state of the selected ones of the plurality of internal signals that match the trigger pattern for later retrieval by the server.

Applicant respectfully submits that claim 1 is, therefore, allowable over Shen.

C. *Other Independent Claims*

Claim 9 incorporates limitations similar to those of claim 1. Claim 9 (and the claims that depend therefrom) are also allowable over Shen for reasons corresponding to those set forth with respect to claim 1.

Applicant submits that claims 1-9, 12, 14-15 and are allowable over the reference cited above, and are in condition for allowance. Should any unresolved issues remain, the Examiner is invited to call the undersigned at the telephone number indicated below.

Respectfully submitted,
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Date

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